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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,157	02/13/2004	Shuji Mayama	118680	4034

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,157	MAYAMA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feb 13 & Jul 9, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. For example, pages 1 (lines 9-11) and 5 (lines 17-18) describe the circuit of Fig. 4 within the Background Art section, and/or as "related art." Fig. 5 shows the current noise with respect to Fig. 4. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because the connection between transistors 28 and 29 in Fig. 2 is not shown. Although it is understood, a line should be shown clearly coupling the drain of transistor 28 to the drain of transistor 29. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is

to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 14, line 3 "FET 3" should be --FET 23--; and "C2" on lines 15 and 18 should be --C4--. Page 18, line 12 "FET 7" should be --FET 27--. These changes will ensure the descriptions correspond to the reference designators "23", "C4", and "27" shown in Fig. 2. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The use of first/second switches, and a follower circuit with a transistor and resistor, as recited within claim 1 imply the transistor and switches are distinct elements. Therefore, the limitations are misleading because the single transistor of claim 1 is actually one

of those switches. Related to this problem, it is not understood how a single transistor is interposed on both the first and second paths as claim 1, lines 31-32 cite.

Also related to the problems described above, claim 2 recites the limitation "the respective transistors" in line 2. There is insufficient antecedent basis for this limitation in the claim because claim 1 only recites a single "transistor."

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadd, in view of Ito et al. (Ito). Fig. 2 of Nadd shows a charge pump circuit comprising first/second diodes 45/46 interposed in series between input portion 49 receiving power source input Vcc and an output portion (e.g. cathode of 46 coupled to the gate of 32) for

outputting a stepped up voltage, wherein the forward direction of each diode is directed to the output portion side; capacitor 44 is interposed between a connecting portion (i.e. cathode) of first diode 45 on the side of the output portion, and ground (via the understood pull-down section of buffer 42); and driver 41 provides a clock signal which allows alternate/opposite phase type operation of buffer 42. Nadd discloses the charge pump "can be of any desired type" on line 25 of column 4, and that high side switching circuits can be used in automotive applications (e.g. see column 3, line 19-22). However, although Nadd shows buffer 42 (that one of ordinary skill in the art would recognize as one type of a pull-up/pull-down circuit), the reference does not clearly show or disclose the first/second switches, and a constant current charging and discharging circuit with a follower circuit. Ito shows one type of pull-up/pull-down buffer device in Fig. 1 with constant current sources 15 and 16. The device allows for switching between high and low levels as high speed, and provides accurate output levels (e.g. see column 2, lines 6-9 and column 4, lines 17-23). As understood from the related waveforms shown in Fig. 3, the device's output signal 22 follows input signal 20 (e.g. when the input signal goes high, the output signal goes high after a slight delay). Therefore, Ito's Fig. 1 circuit is one type of follower circuit. It would have been obvious to one of ordinary skill in the art to replace Nadd's (generic - no details) buffer 42 with Ito's Fig. 1 buffer. With this type of configuration, first switch 4 will conduct and cutoff a connecting path between connecting portion 43 of capacitor 44 and ground; and second switch 3 will conduct and cutoff a connecting path between connecting portion 43 and input portion 49. The first/second switches will conduct alternately in phases opposite to each other with respect to the signal received from driver 41. Ito's circuit 100 can be deemed a constant current charging and discharging circuit using a follower circuit.

Elements 4,6 of the follower circuit are interposed on a first path (e.g. between 12 and 10) through which current flows when first switch 4 conducts, providing a connecting path between connecting portion 43 and ground (which corresponds to Ito's node 10), and current from input portion 49 charges capacitor 44; and elements 3,5 of the follower circuit are on a second path (e.g. between 9 and 12) through which current flows when second switch 3 conducts, providing a connecting path between connecting portion 43 and input portion 49 (which corresponds to Ito's node 9), and capacitor 44 discharges. The follower circuit comprises transistors 4/3 interposed on the first/second paths, respectively for controlling the current amount flowing through those paths, and resistors 6 and 5 are connected in series with respect to their corresponding transistor, on either an upstream or downstream side. Therefore, claim 1 is rendered obvious. The circuit of Ito provides a specific, known type of pull-up/pull-down buffer that can be used in place of Nadd's generic type buffer (e.g. no details are shown or disclosed), wherein the use of the resistors will minimize ringing. Since transistors 4/3 function as first/second switches 4/3, claim 2 is also rendered obvious. Fig. 2 of Nadd shows the output of charge pump circuit 40 being used to drive a gate of FET 32; column 1, lines 11-16 discloses that the gate of a MOS requires a higher potential than the power supply; and column 3, lines 19-22 clearly discloses high side switching circuits can be used in automotive applications. Therefore, claims 3/4 are rendered obvious with respect to the use of the Nadd/Ito charge pump circuit with vehicle mounting, and for driving the gate of a FET. For example, Nadd's FET 32 is driven by charge pump circuit 40, and it controls power source current supplied from power source line Vcc to load 31.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadd, in view of Vajdic et al. (Vajdic). Fig. 2 of Nadd shows a charge pump circuit comprising first/second

diodes 45/46 interposed in series between an input portion (e.g. 49) receiving power source input Vcc and an output portion (e.g. cathode of 46 coupled to the gate of 32) for outputting a stepped up voltage, wherein the forward direction of each diode is directed to the output portion side; capacitor 44 is interposed between a connecting portion (i.e. cathode) of first diode 45 on the side of the output portion, and ground (via the understood pull-down section of buffer 42); and driver 41 provides a clock signal which allows alternate/opposite phase operation of buffer 42. Nadd's Fig. 5 shows constant current discharging circuit 53, with current mirror 61,60, coupled between buffer 42 and ground. This configuration minimizes noise with respect to the charging/ discharging of capacitor 44 (e.g. see a related description on columns 1 (lines 58-61) and 4 (lines 2-6 and 27-31)). Nadd also discloses the charge pump "can be of any desired type" on line 25 of column 4. However, the Nadd reference does not clearly show or disclose the first/second switches, and a constant current charging and discharging circuit. One of ordinary skill in the art would understand that buffer 42 represents one type of pull-up/pull-down device (e.g. a CMOS inverter). Vajdic shows and discloses as least one specific type of pull-up/pull-down device in Fig. 6. Therefore, it would have been obvious to one of ordinary skill in the art to replace Nadd's buffer 42 (of Fig. 2) with Vajdic's Fig. 6 circuit. Vajdic's circuit comprises first switch 53 that will conduct and cutoff a connecting path between connecting portion 43 of Nadd's capacitor 44 and ground; second switch 58 that will conduct and cutoff a connecting path between connecting portion 43 and input portion 49; and elements 55-57,51-52,54 will form a constant current charging and discharging type circuit. Receiving the clock pulses from driver 41, the conduction of the first/second switches will alternate in phases opposite to each other. The constant current...circuit comprises current mirror circuit 55-56,51-52, with: 1) element 52

of current mirror 51-52 being provided in a position on a first path (e.g. between 60 and VSS) that allows current to flow from Nadd's connecting portion 43 (corresponding to Vajdic's node 60) and ground, allowing current from input portion 49 (via 45) to charge capacitor 44; and 2) element 56 of current mirror 55-56 being provided on a second path (e.g. between 60 and Vcc) that allows current to flow between connecting portion 43 and input portion 49 when second switch 58 is conducting, allowing the capacitor to be discharged. Therefore, claim 5 is rendered obvious. Vajdic's circuit provides one known pull-up/pull-down circuit that can replace Nadd's generic buffer 42. Also, it is understood that Nadd's Fig. 5 example shows current source 53 coupled between ground 52 and floating node 51 to provide a constant voltage and minimize noise with respect to those pins, wherein Vajdic's constant current...circuit provides isolation between power source input Vcc and the pin between 56 and 58, and also provides isolation between ground Vss and the pin between 52 and 53. Thus, Vajdic's circuitry will help minimize noise with respect to both the power source side, and the ground side, pins. It would have been obvious to one of ordinary skill in the art to include the Nadd/Vajdic charge pump circuit inside an IC, rendering claim 6 obvious. For example, Nadd discloses the circuit is "integrated into a silicon chip", and it's "integrated into a common semiconductor chip" (e.g. see the abstract, and column 1, lines 5-10). Formed inside an IC, the components will take up less area, be easier to fabricate, and operate under substantially the same conditions (e.g. temperature).

No claim is allowable.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claims. Although not used in any formal rejections described above,

Fig. 1 of Yamaguchi shows a pull-up/pull-down circuit that uses current mirror circuitry to ensure a constant current is provided at its output. Fig. 2 of Pierce et al. shows an example of a pull-up/pull-down circuit comprising resistors 223 and 225 in the current paths of their corresponding transistor/switch 224a and 224b. Yamaguchi's and Pierce et al.'s circuits could replace Nadd's pull-up/pull-down circuit 42 for the same reasoning as applied above with respect to the Nadd/Vajdic and Nadd/Ito et al. rejections, respectively. Therefore, these references should be carefully reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund
20 May 2005

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